PATENT APPLICATION
DOCKET NO.: 100201496-2

REMARKS

Favorable reconsideration of the present application as currently constituted is respectfully requested.

Claims 1-15 are pending, of which claims 1, 8, and 12 are in independent form.

Claims 1 and 6-15 have been amended hereby. No new matter is introduced.

Regarding the Double Patenting Rejection

In the pending Office Action, claims 1-7 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-10 of U.S. Patent No. 6,714,035. Also, claims 8-11 and claims 12-15 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 10-15 and claims 16-21, respectively, of U.S. Patent No. 6,714,035. In response, Applicant has enclosed herewith a terminal disclaimer in accordance with 37 C.F.R. §1.321. Accordingly, Applicant respectfully submits that the pending doubling patent rejection of claims 1-15 has been obviated.

Regarding the Claim Rejections- 35 U.S.C. §102

In the pending Office Action, claims 1-5 are rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 6,177,989 to Bruce (hereinafter "the *Bruce* reference"). The Examiner commented as follows in applying the *Bruce* reference with respect to the §102(b) rejections:

> As to claim 1, Bruce discloses in Fig. 2, 3, a system comprising: a device under test (DUT 200) assembly including said IC, wherein the IC includes at least one node (see figure 2) operable to be stimulated to a stuck-at fault condition by a certain frequency of electromagnetic (EM) radiation (via 252); a probe operable (beam 270, 274) with a laser voltage probe to stimulate the DUT assembly with said frequency of EM radiation; and a test pattern generator (generate the test vectors not shown, see col. 3, lines 25-45) and interface system (inherent) interfacing with the DUT assembly (200), the test pattern generator and interface system operating to apply a test vector to the DUT assembly (col. 3, lines 25-45), means (via detector 260) for comparing the IC's output against expected results associated with the test vectors set; and receive a corresponding response indicative of a fault coverage (via 264).

Applicant respectfully submits that the pending §102(b) rejections have been overcome or otherwise rendered moot by the present response. The present invention, as defined by the currently amended claim 1, is directed to a system for measuring fault coverage in an IC that includes a probe operable to stimulate at least one node of the IC to a temporary stuck-at fault condition with a frequency of electromagnetic radiation. Upon creating a temporary stuck-at fault condition at one or more

nodes, a test pattern generator and interface system applies a test vector to measure fault coverage in the IC.

The *Bruce* reference teaches a system that utilizes laser induced current for semiconductor defect detection. In particular, the *Bruce* reference employs a laser source to generate electromagnetic radiation for detecting short circuits that are already present in a semiconductor device. Applicant's invention, on the other hand, discloses a fault coverage measurement system having a probe that is operable to stimulate node to a temporary stuck-at fault condition with electromagnetic radiation. That is, as will be shown below, the system of the *Bruce* reference detects short circuits in an IC rather than induce temporary stuck-at fault conditions at one or more locations in the IC for coverage measurement.

With reference to FIG. 2 of the *Bruce* reference, a beam 202 of laser light illuminates nodes 204 of a semiconductor structure 200. If a node has a short circuit, a current is induced therein, thereby causing a photo-emission 206 which may be detected by a photo-emission detector 260 in order to produce an image of the integrated circuit 200. The *Bruce* reference describes the detection process as follows:

> FIG. 2 is a perspective view of a semiconductor structure 200 at which a beam 202 of laser light is directed. The dashed line block 204 is an exaggerated depiction of a node within the integrated circuit.

> The beam 202 of laser light, also exaggerated in size, illuminates node 204. If the node has a short circuit, a current is induced therein, thereby causing a photo-emission 206. While not shown, it will be appreciated that some portion of the laser light 202 is also reflected from the integrated circuit 200. It is expected that the photo-emission will have a wavelength of 0.9 to 2 μm for flip chips and will have an intensity that is greatest at about 1.3 μm.
>
> The coordinates of the photo-emission 206 can be mapped to a region of the integrated circuit 200 in order to ascertain the particular circuitry that comprises the node 204. Once the node has been identified, various test vectors can be constructed and applied to exercise the particular circuitry to confirm the defect.
>
> The invention finds use in inspection of both conventional integrated circuit devices, for example, those having the front side exposed, and in flip-chip devices. For conventional devices, the invention can be used to quickly identify the location of a potential defect by scanning the front side of the integrated circuit. The invention is particularly useful for inspecting flip-chip integrated circuits because in such a circuit the front side is obscured from view. Therefore, conventional techniques for visual inspection of the front side of a flip-chip integrated circuit are difficult, if not impossible without destroying the circuit. Column 3, line 45 - column 4, line 6.

Hence, the *Bruce* reference is concerned with employing electromagnetic radiation to detect short circuits in order to inspect and map semiconductor structures. The *Bruce* reference is not concerned with employing electromagnetic radiation to stimulate stuck-at faults in order to measure fault coverage. Further, the *Bruce* reference neither discloses nor suggests a system for measuring fault coverage in an IC that includes a probe operable to stimulate at least one node of the IC to a

temporary stuck-at fault condition with a frequency of electromagnetic radiation as recited by Applicant in claim 1. Accordingly, Applicant respectfully submits that claim 1 is patentable over the *Bruce* reference.

Claims 2-5 depend from base claim 1 and add further limitations thereto. Therefore, it is respectfully submitted that claims 2-5 are also patentable over the *Bruce* reference.

Regarding the Claim Rejections- 35 U.S.C. §103

Claims 6-15 stand rejected in the pending Office Action under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,189,365 to Ikeda et al. (hereinafter "the *Ikeda* reference") in view of the *Bruce* reference as applied above.

With respect to claims 6 and 7, Applicant respectfully points out that these dependent claims incorporate all the limitations of the base claim 1. As explained in detail hereinabove, the *Bruce* reference is deficient as applied against the currently amended base claim 1. Combining the teachings of the *Ikeda* reference is of no avail, however, in this regard for purposes of obviousness. Applicant respectfully submits that the combination of the *Ikeda* and *Bruce* references does not teach or even remotely suggest all the claim limitations of the present invention as currently claimed. Accordingly, it is believed that

claims 6 and 7 are patentable over the *Ikeda* and *Bruce* references.

With respect to base claims 8 and 12, the following comments were provided in the pending Office Action:

> As to claims 8, 12, Ikeda et al. disclose in Fig. 2, Ikeda et al., disclose a method and system for measuring the fault coverage in an IC comprising the steps of: creating a stuck-at fault condition (col. 2, lines 10-12, and lines 48-50) at a select number of nodes associated with the IC; applying a test vector set (col. 2, lines 13-15 and lines 48-50) to the IC upon creating said stuck-at fault condition; comparing the IC's output against expected results associated with said test vector set (col. 2, lines 19-25 and lines 65-69); and determining fault coverage detected by the test vector set (col. 2, lines 20-25, and lines 65-69; col. 3, lines 1-6). Ikeda et al., does not teach the stimulating a select number of node associated with the IC with a certain frequency of electromagnetic (EM) radiation. However, Bruce teaches in Figs. 2-3, the stimulating a select number of node (204 of figure 2) associated with the IC (200 of figure 2) with a certain frequency of electromagnetic (EM) (via 252). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the system of Ikeda et al., and provides the stimulating a select number of node (204 of figure 2) with a certain frequency of electromagnetic (EM via 252) for easily detecting and analyzing each node of the IC in the inspection of the integrated circuit device.

Applicant respectfully submits that these §103 rejections have been overcome or otherwise rendered moot by the present amendment. The currently amended base claim 8 includes creating a temporary stuck-at fault condition at each of a select number of nodes in an IC. Likewise, the currently amended base claim 12 includes means for stimulating a temporary stuck-at fault

condition at each of a select number of nodes associated with an IC with a frequency of EM radiation. Applicant respectfully submits that the combination of the *Ikeda* and *Bruce* references does not disclose or suggest Applicant's invention as currently defined.

The *Ikeda* reference teaches a method of locating a fault in a logic IC device. In particular, the *Ikeda* reference discloses a method for gathering data from a logic IC device and using the gathered data to generate a test data file for performing a fault simulation, wherein stable faults are introduced in logical operation data that serves as input data.

With reference to FIGS. 1 and 2 of the *Ikeda* reference, a logic IC device 20 having a fault is tested by an LSI tester 21 and the results of the test are stored in a test result file 3 which provides a fault location result 4 that includes information on coordinates, type and function of the faulty logic cell. Where a fault test condition is rendered unreliable due to a racing hazard or the like, a fault simulation may be performed by analyzing the fault location result 4 and using a faulty logic operation data file 5 which serves as input data for the fault simulation. Logic operation data contained in the faulty logic operation data file 5 includes simulated (i.e., virtual) stable faults or stuck-at faults at particular logic cells in order to avoid racing hazards. The actual results of

the fault simulation may then be compared to the expected results to provide further information relative to locating the faults in the logic IC. The *Ikeda* reference describes this fault detection process as follows:

> Referring now to FIGS. 1 and 2, a logic IC device 20 in which a fault has actually occurred is tested by an LSI tester 21, and a known AFL (Automatic Fault Location, refer, for example, to "1990 International Test Conference" pp. 860-870) is performed on the basis of its test result (for example, information on input and output values on respective pins of the tested device chip, the number and positions of faulty input and output pins and so on) recorded in a test result file 3 to obtain a fault location result 4 which includes, for example, information on coordinates, type and function of a faulty logic cell, whether the fault has found on the output side or input side of the cell, and so on.
>
> In the test result file 3, there are recorded logical states at respective input and output pins of a logic IC device, not shown, such as a logic LSI device and a logic VLSI device in a tri-state logic which represents logical states by "0", "1" and "X" (unknown).
>
> Then, if there exists an ambiguous fault condition rendered undefinable due to a hazard or the like in the fault location result 4 obtained by producing an unknown output "X" due to hazard in data recorded in the test result file 3 and executing the AFL, one or more "stable" faults F, which are not influenced by hazard or the like, are intentionally produced in logical operation data which is to serve as input data for a fault simulation, later referred to, by a method shown, for example, in FIGS. 3 and 4, and logical operation data including the faults F is stored in a faulty logical operation data file 5. Column 3, line 42 - column 4, line 3.

Accordingly, the *Ikeda* reference discloses a method for locating a fault in a logic IC device that aims to avoid hazards caused by racing, by using virtual stable faults in a logic operation data file pertaining to the logic device. Applicant respectfully submits that the *Ikeda* reference neither discloses nor suggests, either alone or in combination with the *Bruce* reference, the present invention's limitations directed to stimulating a node of an IC device to create thereat a temporary stuck-at fault condition with electromagnetic radiation provided by a probe. Therefore, Applicant respectfully submits that the pending base claims 8 and 12 are patentable over the applied art. *Ikeda* reference.

Dependent claims 9-11 and 13-15 depend from the base claims 8 and 12, respectively, introduce additional limitations therein. Consequently, it is believed that these dependent claims are also patentable over the *Ikeda* and *Bruce* references.

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SUMMARY AND CONCLUSION

In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the outstanding rejections and allow claims 1-15 presented for reconsideration herein. Accordingly, a favorable action in the form of an early notice of allowance is respectfully requested.

Respectfully submitted,

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